REMARKS

This Preliminary Amendment is being filed with a Request for Continued Examination. Please enter the amendment contained herein before examination of the application.

In a Final Office Action mailed on March 27, 2006, claims 1, 2 and 24-26 were rejected under 35 U.S.C. § 102(e) as being anticipated by Gunzelmann; claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gunzelmann in view of Leonida; claims 4-6, 8, 9, 12-14, 18-21 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gunzelmann in view of Leonida and further in view of Silvestri; claims 27 and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gunzelmann in view of Leonida, Silvestri and Dvorak; claims 10, 11, 15, 16, 17 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dvorak in view of Gunzelmann; and claim 27 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gunzelmann in view of Silvestri. The §§ 102 and 103 rejections are addressed below.

Newly-added Claim 29 and §§ 102 and 103 Rejections of Claims 1-9:

The system of independent claim 1 includes a locked loop circuit to indicate a timing between an input signal and an output signal. The system also includes a processor that is coupled to the locked loop circuit to, based on the indication of the timing, control the locked loop circuit and perform at least one other function in the system that is not related to the control of the locked loop circuit.

Contrary to the limitations of independent claim 1, Gunzelmann discloses two DLLs 5 and 6, which are depicted in Fig. 7. Gunzelmann discloses that the DLLs 5 and 6 receive early-late spacings called "Δ1" and "Δ2." In particular, Gunzelmann states, "the microprocessor 2 uses the early-late spacings Δ1 and Δ2 preset by it and the phase angles T1 and T2, respectively, determined by the phase locked loops DLL 1 and DLL 2, respectively, to calculate the optimal phase angle T0." Gunzelmann, 6:55-57. As depicted in Fig. 7, the phase angle T0 is supplied by the microprocessor 2 to an oscillator 3.

However, Gunzelmann fails to teach or even suggest that the microprocessor 2 controls either DLL 5 or 6 based on a timing that is indicated by the DLL 5, 6. Instead, the late-early spacings Δ1 and Δ2, as recited above, are present, or fixed, and thus, are not based on a timing indicated by either DLL 5 or 6. Therefore, Gunzelmann fails to teach or even suggest the

processor of independent claim 1. As such, a *prima facie* case of anticipation has not been set forth for independent claim 1.

Claims 2-9 and newly-added claim 29 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, for at least the reasons that are set forth above, allowance of claims 1-9 and 29 is requested.

§ 103 Rejections of Claims 10-15:

As amended, the locked loop circuit of independent claim 10 includes a delay line to introduce a delay to an input clock signal to produce an output clock signal. An interface of the locked loop circuit is accessible by a processor to regulate the delay to adjust the timing between the input clock signal and the output clock signal based on an indicated phase difference, which is provided by a phase detector.

Contrary to the limitations of amended independent claim 10, Gunzelmann fails to disclose an interface that is accessible by a processor to regulate a delay between input and output clock signals of a delay line to adjust the timing between these signals based on an indicated phase difference that is provided by a phase detector. Instead, as pointed out above in the discussion of independent claim 1, the late-early spacings $\Delta 1$ and $\Delta 2$ that are received by the DLLs 5 and 6 are fixed parameters. Neither DLL 5 or 6, however, includes an interface that is accessible by the microprocessor 2 to adjust timing between input and output clock signals based on an indicated phase difference from the DLL 5 or 6. As such, Gunzelmann fails to disclose the interface of independent claim 10. As conceded by the Examiner, Dvorak fails to teach or suggest the missing claim limitations.

Claims 11-15 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, for at least the reasons that are set forth above, withdrawal of the § 103 rejections of claims 10-15 is requested.

§ 103 Rejections of Claims 16-23:

As amended, the method of independent claim 16 includes using a processor to control a delay that is introduced by a locked loop circuit between input and output signals of the locked loop circuit based on a timing between the input and output signals that is indicated by the locked loop circuit.

Contrary to the limitations of independent claim 16, Gunzelmann fails to teach or even suggest using a processor to control a locked loop circuit, as set forth in independent claim 16. See discussion of independent claims 1 and 10 above. Dvorak fails to supply the missing claim limitations, for at least the reason that Dvorak fails to teach or suggest using a processor to control locked loop circuit.

Claims 17-23 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, for at least the reasons that are set forth above, withdrawal of the § 103 rejections of claims 16-23 is requested.

§ 103 Rejections of Claims 24-28:

As amended, the article of independent claim 24 includes a computer accessible storage medium that stores instructions to, when executed, cause a processor to receive an indication of a phase difference from a locked loop circuit and control a delay introduced by the locked loop circuit between an input signal and an output signal based on the indicated phase difference.

As discussed above, Dvorak fails to teach or suggest a processor controlling a locked loop circuit and thus, fails to teach or suggest the instructions of independent claim 24. Gunzelmann fails to teach or suggest the missing claim limitations, as Gunzelmann fails to teach or suggest instructions that when executed cause a processor to control a delay that is introduced by a locked loop circuit between an input signal and an output signal of a locked loop circuit based on a phase difference indicated by the locked loop circuit. As set forth above, the late-early spacings $\Delta 1$ and $\Delta 2$ are fixed and are not based on an indicated phase difference.

Claims 25-28 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, for at least the reasons that are set forth above, withdrawal of the § 103 rejections of claims 24-28 is requested.

CONCLUSION

In view of the foregoing, withdrawal of the §§ 102 and 103 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0550US).

Respectfully submitted,

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